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FILE 'CAPLUS, INSPEC, JICST-EPLUS' ENTERED AT 13:07:46 ON 27 MAR 2003

L1 17 S 6 NM GATE OXIDE

L2 12 DUPLICATE REMOVE L1 (5 DUPLICATES REMOVED)

L2 ANSWER 10 OF 12 JICST-EPlus COPYRIGHT 2003 JST
ACCESSION NUMBER: 960569079 JICST-EPlus
TITLE: Reduction of Electron Shading Damage by Using Synchronous Bias in Pulsed Plasma.
AUTHOR: HASHIMOTO K; HIKOSAKA Y; HASEGAWA A; NAKAMURA M
CORPORATE SOURCE: Fujitsu Ltd., Kawasaki
SOURCE: Proc Symp Dry Process, (1995) vol. 17th, pp. 33-37. Journal Code: Y0378A (Fig. 11, Ref. 8)
PUB. COUNTRY: Japan
DOCUMENT TYPE: Conference; Article
LANGUAGE: English
STATUS: New
AB A novel method for reducing charging damage from "electron shading" effect is proposed. The concept is to utilize the coolest electrons at the end of the afterglow period of pulsed plasma with the rf bias synchronized at this phase. This concept was examined with an inductively coupled plasma (ICP) apparatus. An exposure to a cw Ar ICP damaged most of MOS capacitors with **6-nm gate oxide** connected to 105 shaded antennas. This damage was reduced only slightly even with the 5-.MU.s on/10-.MU.s off pulse modulation when the rf bias was asynchronous (60kHz). A significant damage reduction was observed with the synchronous rf (66.7kHz) bias of the optimal phase expected. This effect was well correlated with the results of time-resolved probe and optical emission measurements; they indicate that the electron temperature or hot electron density at the phase when the electrons can reach the wafer surface was reduced with this method. (author abst.)

L2 ANSWER 12 OF 12 INSPEC COPYRIGHT 2003 IEE
ACCESSION NUMBER: 1994:4759270 INSPEC
DOCUMENT NUMBER: B9410-2560R-082
TITLE: Ultra-thin gate oxide yield and reliability.
AUTHOR: Depas, M.; Vermeire, B.; Mertens, P.W.; Meuris, M.; Heyns, M.M. (IMEC, Leuven, Belgium)
SOURCE: 1994 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.94CH3433-0)
New York, NY, USA: IEEE, 1994. p.23-4 of xv+168 pp. 7 refs.
Conference: Honolulu, HI, USA, 7-9 June 1994
Price: CCCC 0 7803 1921 4/94/$3.00
ISBN: 0-7803-1921-4
DOCUMENT TYPE: Conference Article
TREATMENT CODE: Experimental
COUNTRY: United States
LANGUAGE: English
AB In this paper we demonstrate that ultra-thin (3-**6 nm**) **gate oxides** with a very good thickness uniformity and a low defect density can be grown by thermal oxidation using a conventional furnace. A strong reduction of the low field MOS leakage current, related to oxide wearout, is observed for thinner oxides and correlates with a dramatic improvement of the TDDB characteristics. It is shown that the voltage scaling of future MOS devices with an oxide thickness less than 5 nm will be determined by the direct tunnel current through the oxide.

L2 ANSWER 11 OF 12 INSPEC COPYRIGHT 2003 IEE
ACCESSION NUMBER: 1995:4881007 INSPEC
DOCUMENT NUMBER: B9503-2570D-019
TITLE: A 0.1 mu m CMOS technology with tilt-implanted punchthrough stopper (TIPS).
AUTHOR: Hori, T. (Central Lab., Matsushita Electr. Ind. Co. Ltd., Kyoto, Japan)
SOURCE: International Electron Devices Meeting 1994. Technical Digest (Cat. No.94CH35706)
New York, NY, USA: IEEE, 1994. p.75-8 of 947 pp. 7 refs.
Conference: San Francisco, CA, USA, 11-14 Dec 1994
Sponsor(s): Electron Devices Soc. IEEE
Price: CCCC 0 7803 2111 1/94/$4.00
ISBN: 0-7803-2111-1
DOCUMENT TYPE: Conference Article
TREATMENT CODE: Practical
COUNTRY: United States
LANGUAGE: English
AB A 0.1- mu m CMOS technology with tilt-implanted punchthrough stopper (TIPS) structure is proposed. By taking advantage of large-angle-tilt implant, the p- and n- TIPS pocket regions are successfully realized adjacent to the n- LDD region and p+ source/drain without increasing impurity concentration under the n+ and p+ source/drain junctions for n- and p-FETs, respectively. In spite of the low 1016cm-3-order substrate doping, deep 0.15-0.2 mu m source/drain, and practically thick **6 -nm gate oxides**, the TIPS n- and p-FETs are for the first time demonstrated to achieve high punchthrough resistance with suppressed body effect and junction capacitance, at least, down to 0.12 mu m and 20-40%, improved switching speed of 20 ps unlike conventional FETs, while maintaining full compatibility with the conventional CMOS process. The TIPS n- and p-FETs also exhibit suppressed hot-carrier-induced degradation due to the confined impurity profiles. The TIPS technology is most promising for 0.1- mu m CMOS ULSIs.

L2 ANSWER 9 OF 12 CAPLUS COPYRIGHT 2003 ACS DUPLICATE 4

ACCESSION NUMBER: 1996:236212 CAPLUS
DOCUMENT NUMBER: 124:329339
TITLE: High performance 0.3 .mu.m CMOS using I-line lithography and BARC
AUTHOR(S): Thakar, G. V.; Madan, S. K.; Garza, C. M.; Krisa, W. L.; Nicollian, P. E.; Wise, J. L.; Lee, C. K.; McKee, J. A.; Appel, A. T.; et al.
CORPORATE SOURCE: Semiconductor Process and Device Center, Texas Instruments, Dallas, TX, USA
SOURCE: Symposium on VLSI Technology, Digest of Technical Papers, 15th, Kyoto, June 6-8, 1995 (1995), 75-6. Business Center for Academic Societies Japan: Tokyo, Japan.
CODEN: 62PWAR
DOCUMENT TYPE: Conference
LANGUAGE: English

AB TiN or org. Bottom AntiReflection Coatings (BARC), polysilicon hammerheads, phase shift masks, quadrupole off-axis illumination I-line lithog. at N.A.=0.60, shallow source/drain extenders, LOCOS isolation, and **6 nm gate oxide** are used to obtain high performance 0.30 .mu.m 2.5 V CMOS with effective channel lengths <0.20 .mu.m. The use of BARC reduces off current and improves PMOS hot carrier reliability.

L2 ANSWER 8 OF 12 CAPLUS COPYRIGHT 2003 ACS DUPLICATE 3

ACCESSION NUMBER: 1995:936760 CAPLUS
DOCUMENT NUMBER: 124:42544
TITLE: Controlled thin oxidation and nitridation in a single wafer cluster tool
AUTHOR(S): Sagnes, I.; Laviale, D.; Glowacki, F.; Blanchard, B.; Martin, F.
CORPORATE SOURCE: France Telecom-CNET, Meylan cedex, 38243, Fr.
SOURCE: Materials Research Society Symposium Proceedings (1995), 387(Rapid Thermal and Integrated Processing IV), 253-8
CODEN: MRSPDH; ISSN: 0272-9172
PUBLISHER: Materials Research Society
DOCUMENT TYPE: Journal
LANGUAGE: English

AB For both advanced MOS technologies (gate length .ltoreq. 0.25 .mu.m) and EEPROMs, the quality and reproducibility of thin dielec. films (< 6 nm) are essential. To obtain such dielecs. involves very precise control of the silicon surface prepn. and gate oxide growth. Furthermore, research into such supplementary properties of oxide as improved SiO2/Si interface resistance to current injections or enhanced p+ gate resistance to boron penetration in the channel may require nitridation treatment. Such a sequence of steps can be carried out under controlled atm. using a cluster tool. This paper presents the preliminary results obtained in a single wafer cluster tool on (i) the surface prepn. under ozone of a silicon wafer immediately after dild. liq. HF treatment and (ii) the nitridation of the **6 nm gate oxide** under low temp., low pressure gaseous NO. It is shown that the NO mol. can be successfully used in Rapid Thermal Processing (RTP) and allows gate oxides to be nitrided with properties at least equiv. to those obtained under N2O nitridation, but with a strikingly reduced thermal budget.

L2 ANSWER 7 OF 12 CAPLUS COPYRIGHT 2003 ACS DUPLICATE 2

ACCESSION NUMBER: 1996:251021 CAPLUS
DOCUMENT NUMBER: 124:329482
TITLE: Impact of negative-bias temperature instability on the lifetime of single-gate CMOS structures with ultrathin (4-**6 nm**) **gate oxides**
AUTHOR(S): Ogawa, Shigeo; Shimaya, Masakazu; Shiono, Noboru
CORPORATE SOURCE: NTT LSI Laboratories, Nippon Telegraph and Telephone Corporation, Kanagawa, 243-01, Japan
SOURCE: Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1996), 35(2B), 1484-90
CODEN: JAPNDE; ISSN: 0021-4922
PUBLISHER: Japanese Journal of Applied Physics
DOCUMENT TYPE: Journal
LANGUAGE: English

AB The lifetime of ultrathin gate oxides under low-field stress conditions has been studied on the basis of empirical acceleration equations for neg.-bias temp. instability (NBTI) up to 5000 h for 4.2-to-30-nm-thick oxides of MOS structures. The derived lifetime, the max. acceptable oxide field, and the max. acceptable operating voltage are found to be strongly dependent on the reliability specification. Since the no. of interface traps induced by NBTI is inversely proportional to the oxide thickness, this instability becomes an important factor limiting the lifetime of single-gate CMOS structures with ultrathin gate oxides.

L2 ANSWER 6 OF 12 INSPEC COPYRIGHT 2003 IEE
ACCESSION NUMBER: 1998:5923955 INSPEC
DOCUMENT NUMBER: B9807-2560R-011
TITLE: Silicon dioxide breakdown induced by SHE (substrate hot electron) injection.
AUTHOR: Umeda, K. (Central Res. Lab., Hitachi Ltd., Kokubunji, Japan); Tomita, T.; Taniguchi, K.
SOURCE: Electronics and Communications in Japan, Part 2 (Electronics) (Aug. 1997) vol.80, no.8, p.11-19. 15 refs.
Published by: Scripta Technica
Price: CCCC 8756-663X/97/080011-09
CODEN: ECJEEJ ISSN: 8756-663X
SICI: 8756-663X(199708)80:8L.11:SDBI;1-O
DOCUMENT TYPE: Journal
TREATMENT CODE: Practical; Theoretical; Experimental
COUNTRY: United States
LANGUAGE: English

AB A gate silicon oxide film breakdown experiment is attempted by SHE (substrate hot electron) injection in an n-channel MOSFET with **6 -nm gate oxide** film, where the reverse bias voltage is impressed on the silicon substrate to inject the high-energy electron into the gate electrode side. Examining the difference from the QBD value (cumulative charge density to breakdown) in Fowler-Nordheim injection, several points are revealed. The high-energy electron injected from the silicon substrate side breaks the valence bond in the gate oxide film, and, forming a chain, the breakdown of the oxide film occurs by short-circuiting the substrate and the gate electrode. This differs from previously reported models, such as hole injection from the anode or nonuniformity of the oxide film. It is also noted that the oxide film breakdown by this injection mechanism is a local breakdown, with a breakdown diameter of 10 to 30 nm.

L2 ANSWER 5 OF 12 INSPEC COPYRIGHT 2003 IEE
ACCESSION NUMBER: 1998:5932158 INSPEC
DOCUMENT NUMBER: B9807-2570D-022
TITLE: 0.25 mu m CoSi2 salicide CMOS technology thermally stable up to 1000 degrees C with high TDDB reliability.
AUTHOR: Ohguro, T.; Nakamura, S.; Morifuji, E.; Yoshitomi, T.; Morimoto, T.; Harakawa, H.; Momose, H.S.; Katsumata, Y.; Iwai, H. (Toshiba Corp., Kawasaki, Japan)
SOURCE: 1997 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.97CH36114)
Tokyo, Japan: Japan Soc. Appl. Phys, 1997. p.101-2 of xv+162 pp. 3 refs. Availability: Business Center for Academic Societies Japan, 5-16-9 Honkomagome, Bunkyo-ku, Tokyo 113, Japan
Conference: Kyoto, Japan, 10-12 June 1997
ISBN: 4-930813-75-1
DOCUMENT TYPE: Conference Article
TREATMENT CODE: Experimental
COUNTRY: Japan
LANGUAGE: English
AB Summary form only given. The thermal stability of 0.25 mu m CoSi2 CMOS has been investigated. By choosing the SiO2 gate cap at the Si3N4 sidewall RIE and in-situ phosphorus doped poly Si as the gate electrode, it has been confirmed that there is no degradation in the resistance of 0.15 mu m width CoSi2 gate electrode, in the TDDB of **6 nm gate oxide**, and in the leakage current of a reverse biased diode, after 1,000 degrees C, 20 s nitrogen anneal. This is an adequate margin for the CoSi2 CMOS at the process temperature. Thus, CoSi2 CMOS can be applied to a wide range of applications with different process requirements.